REMARKS

35 USC 102(e) Rejection: (Claims 1-22)

In section 2 of the office action, the examiner noted that: Claims 1-22 are rejected under 35 USC 102(e) as being anticipated by Madurawe (US 6,747,478).

In the current application, the applicant discloses techniques to construct programmable wire structures for structured array integrated circuits. The wire structure comprises a switch & configuration circuit, both fabricated above a metal layer to facilitate metal wire connections. In contrast, Madurawe US 6,747,478 discloses a novel programmable logic device wherein the programmable logic content (namely the switch) is located below any metal layers while the configuration circuit may be located above metal. In both cases the applicant identifies a method to replace memory based configuration circuits with hard-wires to convert programmable devices to hard-wired devices. In the former (current application), this conversion is done by replacing only the configuration circuit (not the switch) with hard-wires, while in the latter (US 6,747,478) both configuration circuit and the switch are replaced by hard-wires. These differences are further illustrated below to demonstrate that they are patentably distinguishable.

There are 3 independent claims in the current application. They are:

1. (Original) A programmable wire structure for an integrated circuit, comprising:
a programmable switch coupling two nodes, said switch having a first state that connects said two nodes, and said switch having a second state that disconnects said two nodes; and
a configuration circuit coupled to said programmable switch, said circuit comprising a means to program said switch between said first and second state; and
a first metal layer fabricated above a silicon substrate layer, said switch and said configuration circuit fabricated substantially above said first metal layer.

11. (Previously presented) A wire structure for an integrated circuit having two selectable methods of connecting wires, comprising:
a first selectable method comprising programmable switches, each said switch coupling a wire in a first set to a wire in a second set, and said method providing a means to program a user defined interconnect pattern between said first and second set of wires; and
a second selectable method comprising permanent connections, each switch in said first selectable method replaced by a connected or a disconnected wire, said permanent connection pattern duplicating one of said user defined interconnect patterns.

18. (Original) A semiconductor device for integrated circuits with two selectable

manufacturing configurations, comprising:
a first module layer having an array of structured cells, said module layer having at least one layer of metal; and
a second module layer formed substantially above said first module layer comprising two selectable configurations, wherein:
in a first selectable configuration a programmable interconnect structure is formed to connect said structured cells, and
in a second selectable configuration a customized interconnect structure is formed to connect said structured cells.

There are 2 independent claims in US 6,747,478. They are listed below for reference:

1. A three-dimensional semiconductor device with two selectable manufacturing configurations, comprising:
a first module layer having a plurality of circuit blocks; and
a second module layer formed substantially above the first module layer, wherein in a first selectable configuration a plurality of memory circuits are formed to store instructions to control a portion of the circuit blocks, and wherein in a second selectable configuration a predetermined conductive pattern is formed in lieu of the memory circuit to control substantially the same portion of the circuit blocks.

23. A programmable logic device, comprising:
one or more digital circuits formed on a substrate; and
a non-planar circuit electrically coupled to the digital circuits, the non-planar circuit being either a memory constructed to store data to define the logic outputs of the digital circuits to fabricate a field programmable gate array (FPGA) or a conductive pattern constructed to define the logic outputs of the digital circuits to fabricate an application specific integrated circuit (ASIC), wherein the memory and the conductive pattern options have substantially matching functionality and timing characteristics.

There are five fundamental differences between the two inventions that make them patentably distinguishable. The difference between configuration circuit (memory or conductive pattern) and the switch is elucidated first. In the current application, the configuration circuits are defined on page 21, starting at line 6 as follows:

"The term configuration circuit includes one or more configurable elements and connections that can be programmed for controlling one or more circuit blocks in accordance with a predetermined user-desired functionality. The configuration circuit includes the memory element and the access circuitry, herewith called memory circuitry, to modify said memory element. Configuration circuit does not include the logic pass-gate controlled by said memory element".

The applicant further denotes a switch as presented on page 7, starting at line 22 as:

"Four exemplary methods of programmable point to point connections synonymous with programmable switches, between node A and node B are shown in Fig-2. These form connections 110 in Fig-1B where node A is located in a first wire and node B is located in a second wire. A configuration circuit to program the connection is not shown in Fig-2".

And further on page 12, starting at line 18 as:

"Most common switch is a pass-gate device. A pass-gate is an NMOS transistor, a PMOS transistor or a CMOS transistor pair that can electrically connect two points. Other methods of connecting two points include fuse links and anti-fuse capacitors. Yet other methods to connect two points may include an electrochemical cell. Programming these devices include forming one of either a conducting path or a non-conducting path".

As defined above, the applicant has separated the configuration circuit from the switch as two separate entities. (This is identical with the issued patent). With reference to Fig-3B, the switch is the NMOS pass-gate 310, while the configuration circuit is the SRAM circuitry 350 (also detailed in Fig-3A). The five different cases are presented next, with examples of the significance of the differences.

Case-1: The location of the switch is significantly different between the current application, and the issued patent US 6,747,478. In the current application, the switch is above one or more metal layers (ref. Fig-11) while in US 6,747,478 the switch is below all metal layers (ref. Figs. 1, 2, 3 & 4 wherein the switch is part of logic circuits). This difference can be further seen in the current application Fig-6 (in this figure, the switch is made of TFT transistors located in module 652 above the substrate circuits 650 comprising a metal layer), and the US 6,747,478 Fig-4 (in this figure, only configuration circuits comprising SRAM is located in module 152, while the NMOS switch resides in the substrate layer 150). This difference and motivation for change is further described on page 27, starting at line 16 in the current application as:

"New programmable logic devices utilizing thin-film transistor configurable circuits are disclosed in incorporated by reference Application Serial No. 10/267,483, Application Serial No. 10/267,484 and Application Serial No. 10/267,511. Those three disclosures describe a programmable logic device and an application specific device fabricated from the same base Silicon die. The PLD is fabricated with a programmable memory module, while the ASIC is fabricated with a conductive pattern in lieu of the memory. Both memory module and conductive pattern provide identical control of logic circuits that are formed on a substrate layer. For each set of programmable memory bit patterns, there is a unique conductive pattern to achieve the same underlying logic functionality. The vertical integration of the configuration circuit leads to a significant cost reduction for the PLD, and the elimination of TFT memory for the ASIC allows an

additional cost reduction for the user. In the three disclosures, the pass-gate connecting device is fabricated on substrate silicon and only the configuration circuit is fabricated in TFT layers. Such construction helps to keep the speed path of timing circuits completely unchanged between the programmable and the customized options. For some multi metal devices, constructing a wire connecting pass-gate in silicon substrate is constrictive. A wire from an upper metal has to reach the silicon substrate many layers vertically below, taking up extra vertical connections in addition to occupying substrate silicon area for the pass-gate. Present novel Programmable Structured Array disclosure describes a programmable wire structure that combines both pass-gate connecting device and configuration circuit into one replaceable TFT module. Furthermore, the methodology disclosed is easily extendable to a plurality of programmable TFT modules sandwiched between multiple pairs of metal layers".

Please note that App. No. 10/267,511 is now US 6,747,478. A process sequence that defines the current application is very different from a process sequence that defines US 6,747,478. Such a process sequence in the current application is shown in Fig-7. Specifically Fig-7.1 illustrates the NMOS TFT layers deposited above 2 layers of metal. Further in Fig-7.2, the center most switch is shown to couples two metal lines, one above and one below. Such a process must have TFT process steps compatible with the metal layers underneath. In contrast US 6,747,478 has the switch within the module layer 1, (102 in Fig-1, 122 in Fig-2 & 3, 150 in Fig-4) below the routing layers 110, 126 & 154 respectively. There is no NMOS TFT requirement for the switch with this arrangement.

Case-2: The conversion of the switch from memory to hard-wire configuration circuits is significantly different between the current application, and the issued patent US 6,747,478. There are two fundamental differences associated with this case.

Case-2.1: In the current application, the switch is replaced by a hard-wires either connected or disconnected. This is shown in the two figures 7.6 and 7.7 respectively. In Fig-7.6, the center switch that couples the lower metal to the upper metal is replaced by a metal wire in Fig-7.7. This is further shown in Fig-9. Fig-9A shows the memory configuration, while Fig-9B & 9C show the possible hard-wire configurations. In contrast, in US 6,747,478 the memory configuration is shown in Fig-14 while the hard-wire configuration is shown in Fig-16. In both, the NMOS switch 360 is present. Only configuration circuit is altered.

Case-2.2: In the current application, the memory aspect of the configuration circuit is obliterated during the conversion from memory circuits to hard-wire circuits. This is shown in Fig-9. Fig-9A shows the memory configuration, while Fig-9B & 9C show the possible hard-wire

configurations. In Fig-9B & 9C, there is no need for the memory aspect to be retained, and none is shown. In contrast, in US 6,747,478 the memory configuration is shown in Fig-14 while the hard-wire configuration is shown in Fig-16. In Fig-16, the memory aspect of the configuration 362 is retained, with connections to either Vcc or Vss to mimic a memory output.

Case-3: Maintaining the switch transient timing delay during the conversion from memory to hard-wire configuration circuits is significantly different between the current application, and the issued patent US 6,747,478. In the current application, the hard-wire is selected to have a resistance that is similar to the ON resistance of the TFT transistor it replaces. The signal traverses the NMOS switch in the first case, and it traverses the metal-link in the second case. Thus the time constant represented by "RC" component has to be matched. This resistance matching is fully described on page 42, line 6 thru page 43, line 10 of the current application. Such limitations and careful calculations are completely unnecessary in US 6,747,478. Further the knowledge is not explicitly or impliedly stated either. The replacement of memory circuit with hard-wire configuration occurs without change to NMOS pass-gate, and hence the signal path. The I_1 to O_1 delay between Fig-14 and Fig-16 remain identical. Hence the timing is 100% identical between the two options.

Case-4: The current application allows insertion of switches above any metal layer (not necessarily only the first metal) in the metal structure, very different from the single switch location imposed in US 6,747,478. This is described in page 28, line 13, and listed here under Case-1 above. The value of such a concept is to optimize the metal connectivity with the most suitable location. In the issued patent US 6,747,478, there is only one location for the switch, namely the substrate layer. All wires have to jog down to the substrate to connect to the switch making interconnect very restrictive, and consume a larger area.

Case-5: The current application allows insertion of switches between any two metal layers, in more than one location of the metal structure, very different from the single switch location imposed in US 6,747,478. This is described in page 28, line 13, and listed here under Case-1 above. The scalability of such a concept leads to a hierarchy of metal connectivity regions. In the issued patent US 6,747,478, there is only one location for the switch, namely the substrate layer. All wires have to jog down to the substrate to connect to the switch making interconnect very restrictive, and consume a larger area.

A) Claim-1 rejection:

A1) A first basis to traverse the rejection is in the position of the switch between the two disclosures (Case-1). In the current application, the switch is above a metal layer. This can be seen in the claim language as shown below:

Re. claim 1: "a first metal layer fabricated above a silicon substrate layer, said switch and said configuration circuit fabricated substantially above said first metal layer".

In contrast, both independent claims of US 6,747,478 describe a structure wherein the switch is below a metal layer, positioned alongside of logic transistors. Only the configuration circuit (either as memory circuit or as conductive pattern is constructed above metal layers. This can be seen in the claim language as shown below.

Re. claim 1: "a first module layer having a plurality of circuit blocks; and a second module layer formed substantially above the first module layer, wherein in a first selectable configuration a plurality of memory circuits are formed to store instructions to control a portion of the circuit blocks ...".

Re. claim 23: "one or more digital circuits formed on a substrate; and a non-planar circuit electrically coupled to the digital circuits, the non-planar circuit being either a memory constructed to store data to define the logic outputs of the digital circuits ...".

A2) A second basis to traverse the rejection is in the ability to integrate the switch above any metal layer in the current application (Case-4). In US 6,747,478 there is only one location for this, which was shown to be restrictive in the interconnect efficiency.

A3) A third basis to traverse the rejection is in the ability to integrate multiple levels of switches to connect metal layers in the current application (Case-5). In US 6,747,478 there is only one location for this, which was shown to be restrictive in the interconnect efficiency.

B) Claim-11 rejection:

B1) A first basis to traverse the rejection is in the conversion of the switch between memory and hard-wire options (Case-2.1). In the current application, the switch is replaced by a metal link, either connected or disconnected. In US 6,747,478 the switch is NOT replaced by a metal link. This can be seen in the claim language as shown below.

Re. claim 11: "switch in said first selectable method replaced by a connected or a disconnected wire".

In contrast, both independent claims of US 6,747,478 describe a structure wherein the switch is below the metal layer, positioned alongside of logic transistors. Only the configuration circuit (either as memory circuit or as conductive pattern) is constructed above metal layers. This can be seen in the claim language as shown below.

Re. claim 1: "a first module layer having a plurality of circuit blocks; and a second module layer formed substantially above the first module layer, wherein in a first selectable configuration a plurality of memory circuits are formed to store instructions to control a portion of the circuit blocks ...".

Re. claim 23: "one or more digital circuits formed on a substrate; and a non-planar circuit electrically coupled to the digital circuits, the non-planar circuit being either a memory constructed to store data to define the logic outputs of the digital circuits ...".

B2) A second basis to traverse the rejection is in the elimination of the memory aspect of the configuration circuit during the conversion from memory to hard-wire options (Case-2.2). In the current application, the metal link alleviates the need for memory type control logic. In US 6,747,478 the memory aspect is retained by metal links to Vcc & Vss (see Fig-16).

B3) A third basis to traverse the rejection is in the switching signal delay matching between the conversion from memory to hard-wire options (Case-3). In the current application, the metal link has to be optimized to match the resistance with the switch ON resistance. In US 6,747,478 no resistance matching is required.

B4) A fourth basis to traverse the rejection is in the ability to integrate the switch above any metal layer in the current application (Case-4). In US 6,747,478 there is only one location for this, which was shown to be restrictive in the interconnect efficiency.

B5) A fifth basis to traverse the rejection is in the ability to integrate multiple levels of switches to connect metal layers in the current application (Case-5). In US 6,747,478 there is only one location for this, which was shown to be restrictive in the interconnect efficiency.

C) Claim-18 rejection:

C1) A first basis to traverse the rejection is in the position of the switch between the two disclosures (Case-1). This can be seen in the claim language as shown below.

Re. claim 18: "a first module layer having an array of structured cells, said module layer having at least one layer of metal; and a second module layer formed substantially above said first module layer comprising two selectable configurations".

In contrast, both independent claims of US 6,747,478 describe a structure wherein the switch is below the metal layer, positioned alongside of logic transistors. Only the configuration circuit (either as memory circuit or as conductive pattern is constructed above metal layers. This can be seen in the claim language as shown below.

Re. claim 1: "a first module layer having a plurality of circuit blocks; and a second module layer formed substantially above the first module layer, wherein in a first selectable configuration a plurality of memory circuits are formed to store instructions to control a portion of the circuit blocks ...".

Re. claim 23: "one or more digital circuits formed on a substrate; and a non-planar circuit electrically coupled to the digital circuits, the non-planar circuit being either a memory constructed to store data to define the logic outputs of the digital circuits ...".

C2) A second basis to traverse the rejection is in the conversion of the switch between memory and hard-wire options (Case-2.1). In the current application, the switch is replaced by a metal link, either connected or disconnected. In US 6,747,478 the switch is NOT replaced by a metal link.

C3) A third basis to traverse the rejection is in the elimination of the memory aspect of the configuration circuit during the conversion from memory to hard-wire options (Case-2.2). In the current application, the metal link alleviates the need for memory type control logic. In US 6,747,478 the memory aspect is retained by metal links to Vcc & Vss (see Fig-16).

C4) A fourth basis to traverse the rejection is in the switching signal delay matching between the conversion from memory to hard-wire options (Case-3). In the current application,

the metal link has to be optimized to match the resistance with the switch ON resistance. In US 6,747,478 no resistance matching is required.

C5) A fifth basis to traverse the rejection is in the ability to integrate the switch above any metal layer in the current application (Case-4). In US 6,747,478 there is only one location for this, which was shown to be restrictive in the interconnect efficiency.

C6) A sixth basis to traverse the rejection is in the ability to integrate multiple levels of switches to connect metal layers in the current application (Case-5). In US 6,747,478 there is only one location for this, which was shown to be restrictive in the interconnect efficiency.

Each rejected claim in the current application is shown to have a plurality of patentably distinguishable differences with the sited prior art. Each independent claim is also shown to comprise claim elements that are missing from the sited prior art. Case-1 thru Case-5 listed above show the innovative differences in the current application compared to the sited prior art. The US 6,747,478 disclosure lacks explicit or implied references or teachings on these five listed cases. Therefore all independent claims in the current application, claims 1, 11 & 18 and those dependent thereupon (all claims 1-22) are patentably distinguishable from US 6,747,478. Withdrawal of the obviousness-type double patenting rejection of claims 1-22 is respectfully requested.

Examiners Comments:

In Re. sec-3 (with respect to claim 1), the examiner noted: "a first metal layer (126, figure 3) fabricated above a silicon substrate layer, said switch and said configuration circuit fabricated substantially above said first metal layer."

This is incorrect. The switch (which is the transistor in Fig-9) is located in the programmable logic block 124 located in module 122 (figure-3) below the metal layers. The location of programmable logic is stated as module layer 1 in the summary section on Col 2, line 46-53. Said switch IS NOT fabricated substantially above a metal layer.

Withdrawal of the rejection is respectfully requested.

In Re. sec-12 (with respect to claim 11), the examiner noted: "and a second selectable method comprising permanent connections in lieu of said switches, said permanent connection pattern duplicating one of said user defined interconnect patterns (ASIC section, column 5, lines 54-55)."

This is incorrect. Please note the amended Claim 11 filed with the last response. Claim 11 should read: "and a second selectable method comprising permanent connections, each switch in said first selectable method replaced by a connected or a disconnected wire, said permanent connection pattern duplicating one of said user defined interconnect patterns".

The switch in the first selectable method IS NOT replaced by a connected or a disconnected wire. The switch is located in the circuit blocks (circuit blocks include programmable logic blocks) 124 located in module 122 (figure-3) below the metal layers. The location of programmable logic is stated in the summary section on Col 2, line 46-53. Only the configuration circuits in 130 (Fig-3) are replaced by hard-wires, as stated in Col 5, line 54.

Withdrawal of the rejection is respectfully requested.

In Re. sec-14 (with respect to claim 18), the examiner noted: "a first module layer having an array of structured cells (122), said module layer having at least one layer of metal; and a second module layer (126) formed substantially above said first module layer comprising two selectable configurations, wherein: in a first selectable configuration a programmable interconnect structure (figure 14) is formed to connect said structured cells, and in a second selectable configuration a customized interconnect structure is formed to connect said structured cells."

This is incorrect. First, the structured cells 122 were not specified to comprise a metal layer. As stated in Col 14, lines 8-10, only digital circuits are fabricated in 122. These digital circuits may comprise only transistors.

Second, the module layer 126 (in Fig-2 & 3) has only ONE configuration – not TWO configurations. It is the module layer 130 (in Fig-2 & 3) that has two selectable configurations. Circuits in module layer 130 control circuits in module layer 122. This is stated in Col 5, line 32 & Col 5, line 58.

Third, programmable interconnect structure in figure 14 does NOT reside in module 126. The metal wires I_1 & O_1 in figure 14 are located in module 126. The NMOS pass-gate in figure 14 is located in module 122 with digital circuits, and NOT in module 126. The SRAM

configuration element & associated circuitry is located in module 130, and NOT in module 126. Figure 14 cannot be construed as a first selectable configuration for the module layer 126.

Fourth, the customized interconnect structure as shown in figure 16 does not reside in module 126 either. The metal wires I_1 & O_1 in figure 16 are located in module 126. The NMOS pass-gate in figure 16 is located in module 122 with digital circuits, and NOT in module 126. The hard-wired substitution 362 may or may not reside in module 126 based on how the conversion is achieved. As NMOS gate does not belong to module 126, Figure 16 cannot be construed as a second selectable configuration for the module layer 126.

Withdrawal of the rejection is respectfully requested.

Allowable subject matter:

Dependent Claim-23 objection: With respect to Applicant's claim 23, in the Office Action, section 18, the examiner noted that:

> "Claim 23 is objected as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims."

The Applicant has herewith presented arguments as to why all rejected claims 1-22 are distinctly different from US 6,747,478 sited in the office action. Withdrawal of those rejections was requested, and if granted, would absolve the objection to Claim-23. Withdrawal of the objection by the examiner, in view of the requested withdrawal of Claims 1-22 rejections, is respectfully requested.

In summary, the Applicant submits that all claims as presented in this response are allowable in view of the Madurawe US 6,747,478 prior art sited by the examiner, and withdrawal of all objections and rejections is respectfully requested.

CONCLUSION

The applicant believes that the above submission is fully responsive to the office action.

If for any reason the Examiner believes that a telephone conference would in any way expedite this matter, the Examiner is invited to telephone the Inventor Mr. Madurawe at (408) 737-8868 or on his cell phone at (408) 431-5367.

Respectfully submitted,

Raminda Madurawe

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Applicant